REMARKS

The final Office Action mailed December 20, 2002 has been carefully reviewed and the foregoing requested amendments and the following remarks are made in response thereto.

Claims 56-67 have been withdrawn from consideration for allegedly being directed to an invention that is independent or distinct from the invention originally claimed. Claims 41-43, 45-47 and 49-54 stand rejected under 35 U.S.C § 102(b) as being anticipated by U.S. Patent No. 5,239,197 to Yamamoto. Claims 21, 28 and 35 have been allowed. Claims 44, 48 and 55 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the features of the base claim and any intervening claims.

By this amendment, claims 41, 42, 44, 47, 48 and 55 have been amended to further defined the subject matter Applicant regards as the invention. Claim 43 has been rewritten in independent form to include all of the features of amended claim 41. Claims 45, 46, and 49-54, as well as allowed claims 21, 28 and 35, remain unchanged. Thus, claims 21, 28, 35 and 41-55 are presently pending in this application for consideration.

Applicant respectfully submits that independent claims 41-43 are patentably distinguishable over the cited reference as required by §102. Applicant further submits that the cited reference fails to disclose or suggest "a second well region of the first conductivity type formed in each of the at least two first well regions" as recited in independent claims 41-43. Thus, independent claims 41-43 and all claims dependent directly or indirectly therefrom are allowable. This distinction will be described in greater detail below.

THE CLAIMS DISTINGUISH OVER THE CITED REFERENCE

Claims 41-43, 45-47 and 49-54 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamamoto. Although both Applicant's claimed invention and Yamamoto relate generally to a semiconductor integrated circuit device having a plurality of functioning devices on a single substrate, the two address different problems and, not surprisingly, describe different solutions.

Yamamoto is concerned with problems created by short channel effects with high latch-up resistance and increased breakdown voltage between devices when plural devices are provided on a single substrate. To address these problems, Yamamoto discloses in FIGS. 1-4 a substrate (21) of a first conductivity type, at least two first well regions (22, 24, 26) of a second conductivity type, and one second well region (25) of the first conductivity type. As illustrated in the figures, sole second well region (25) is disposed in first well region (24). *See, Yamamoto, column 3, line 50 – column 4, line 40.*

Unlike Yamamoto, Applicant's claimed invention is not directed to reducing short channel effects and the breakdown voltage between devices, but rather is directed to the problem of measuring the characteristics of the plurality of devices. *Specification, page 3, lines 1-13.* According to one embodiment of the present invention, the semiconductor integrated circuit includes a semiconductor substrate of a first conductivity type. At least two first well regions of a second conductivity type are formed separately in the semiconductor substrate and at least one second well region of the first conductivity type is formed in each of the at least two first well regions. The semiconductor integrated circuit device has semiconductor elements formed in the at least two first well regions and the at least one second well region and a memory circuit includes the semiconductor elements.

According to another embodiment of the present invention, integrated circuits are formed on the at least two first well regions, respectively, and have different functions.

Independent claims 41-43 specifically recite the arrangement of "a second well region of the first conductivity type formed in each of the at least two first well regions". Applicant respectfully submits that Yamamoto fails to disclose or suggest this claimed arrangement. Yamamoto merely discloses one second well disposed in one of the first well regions. In the absence of this claimed arrangement, the Yamamoto patent cannot anticipate nor even render obvious the subject matter recited in independent claims 41-43. Thus, independent claims 41-43 are allowable. Moreover, since independent claims 41-43 are allowable, the claims dependent therefrom, namely claims 45-55 are allowable by virtue of their dependence from allowable claims 41-43 and for containing other patentable features. Further remarks regarding the asserted relationship between the

claims and the cited reference are not necessary in view of their allowability. Applicant's silence as to the Examiner's comments is not indicative to the stated grounds of rejection.

CONCLUSION

In view of the foregoing requested amendments and remarks, Applicant respectfully submits that the application is in condition for allowance and requests early notice to that effect.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Washington, D.C. telephone number 202 637-3515 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

HOGAN & HARTSON, L.L.P

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By: _____

Sterlon R. Mason
Registration No. 41,179
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213 337-6700 (Los Angeles, CA)
Phone: 202 637-3515 (Washington, D.C.)
Fax: 213 337-6701
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Version with markings to show changes made:

IN THE CLAIMS:

41. (Once Amended) A Semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

at least one second well region of the first conductivity type formed in each of the at least two first well regions[,]; and

semiconductor MOSFET elements formed in the at least two first well regions and the at least one second well region,

wherein a memory circuit comprises the semiconductor MOSFET elements.

42. (Once Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate; [and]

a second well region of the first conductivity type formed in each of the at least two first well regions;

integrated circuits which are formed on the at least two first well [region] regions and the second well region, respectively, and which have different functions.

43. (Once Amended) [The] A semiconductor integrated circuit device [according to claim 42, wherein] comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed separately in the semiconductor substrate;

a second well region of the first conductivity type [is] formed in [at least one] each of the at least two first well regions; [, and]

a third well region of the second conductivity type formed in each of the at least two first well regions; and

[one of] integrated circuits [is] formed on [the at least one] each of the at least two first well regions [and] , the second well region and the third well region

~~44. (Once Amended) The semiconductor integrated circuit device according~~ to claim 42, wherein a second well region of the first conductivity type having a third well region of the second conductivity type formed therein [is], formed in [at least one] each of the at least two first well regions[,] ; and

one of the integrated circuits [is] formed in the [at least one] each of the at least two first well regions, the second well region and the third well region.

47. (Once Amended) The semiconductor integrated circuit device according to claim 43, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region and the third well region.

48. (Once Amended) The semiconductor integrated circuit device according to claim 44, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region and the third well region.

55. (Once Amended) The semiconductor integrated circuit device according to [claim 44] claim 43, wherein a back gate bias is supplied to the at least two first well regions, the second well region and the third well region, and an input/output circuit or an interface circuit is formed in the at least two first well regions, the second well region and the third well region [and the second well region in which the third well region is formed].